2.7W Stereo Audio Power Amplifier with 4 Selectable Gain Setups and Input MUX AA4006

General Description

The AA4006 is a Class AB stereo audio power amplifier with headphone driver, which can deliver 2.7W into 3Ω speakers with 5.0V power supply and THD+N less than 10%. It is designed specially for notebook PC and portable media player applications.

The AA4006 features stereo full differential input or 2 sets of stereo single-ended audio input. There are 4 different gain settings at BTL mode -6dB, 10dB, 15.6dB and 21.6dB, changed by setting GAIN0, GAIN1 pins. At SE mode, the gain is fixed 4.1dB.

The AA4006 can amplify square waveform beep input signal from BEEP_IN pin and its' output can always reach BTL terminal, masking all other audio inputs regardless of whether the chip is in shutdown, SE or BTL mode.

The AA4006 is available in TSSOP-24 (EDP) package .

Features

- Output Power, THD+N=10%:
  110mW at SE mode for 32Ω Headphone
  220mW at SE mode for 16Ω Headphone
  1.5W at BTL mode for 8Ω Speaker
  2.3W at BTL mode for 4Ω Speaker
  2.7W at BTL mode for 3Ω Speaker
- Supply Voltage Range: 4.5V to 5.5V
- 4 Selectable Internal Fixed Gain Setups
- Stereo 2:1 Input Multiplexer
- Stereo Full Differential Input
- PC Beep Input
- Low Power Consumption at Shutdown mode 150μA Typical
- Excellent Click/Pop Noise Suppression
- Thermal Shutdown Protection
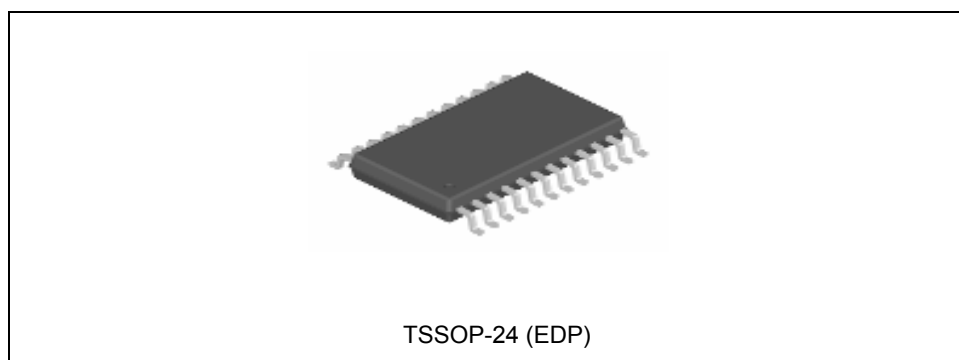
Applications

- Notebook PC
- Portable Media Player

TSSOP-24 (EDP)

Figure 1. Packages Type of AA4006

2.7W Stereo Audio Power Amplifier with 4 Selectable Gain Setups and Input MUX AA4006

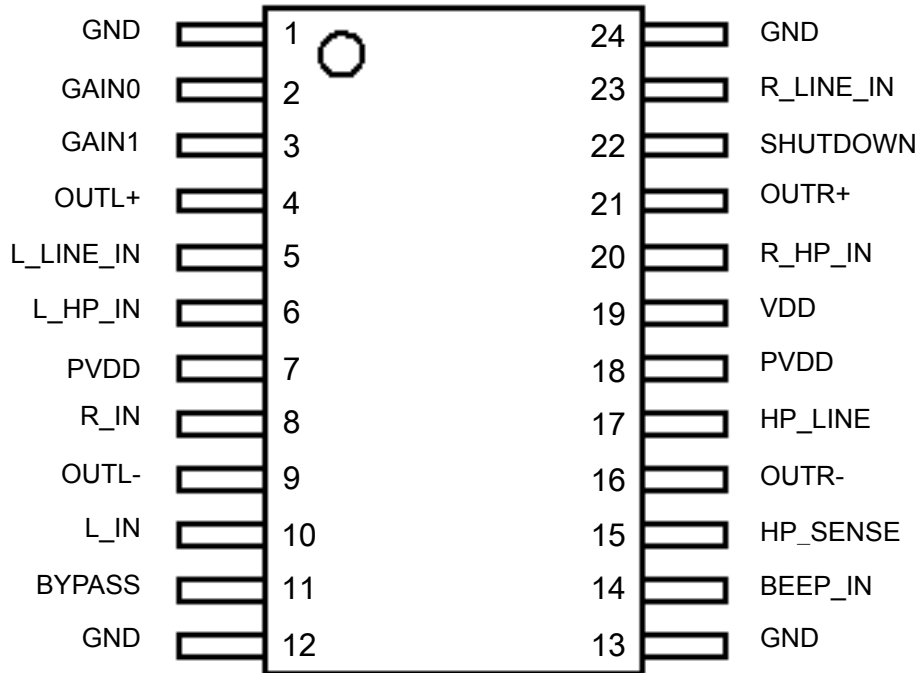## Pin Configuration

G Package

(TSSOP-24 (EDP))

GND	1		24	GND
GAIN0	2		23	R_LINE_IN
GAIN1	3		22	SHUTDOWN
OUTL+	4		21	OUTR+
L_LINE_IN	5		20	R_HP_IN
L_HP_IN	6		19	VDD
PVDD	7		18	PVDD
R_IN	8		17	HP_LINE
OUTL-	9		16	OUTR-
L_IN	10		15	HP_SENSE
BYPASS	11		14	BEEP_IN
GND	12		13	GND

Figure 2. Pin Configuration of AA4006 (Top View)

2.7W Stereo Audio Power Amplifier with 4 Selectable Gain Setups and Input MUX AA4006

Pin Description

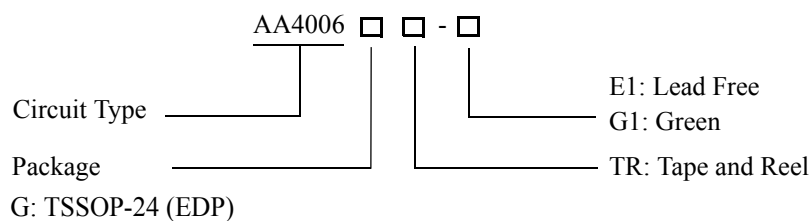| Pin Number	Pin Name	Function
1, 12, 13, 24	GND	Ground reference, it is better to connect with thermal pad
2	GAIN0	Internal gain setup 0, see table 1 below
3	GAIN1	Internal gain setup 1, see table 1 below
4	OUTL+	Left channel positive output
5	L_LINE_IN	Left channel line input
6	L_HP_IN	Left channel headphone input
7, 18	PVDD	Power supply for output stage
8	R_IN	Right channel common input for differential input, AC ground for single-ended input
9	OUTL-	Left channel negative output
10	L_IN	Left channel common input for differential input, AC ground for single-ended input
11	BYPASS	Internal reference voltage pin, connect a 1.0μF ceramic capacitor to GND
14	BEEP_IN	Beep signal input pin
15	HP_SENSE	SE, BTL mode switch pin, L – BTL mode, H – SE mode
16	OUTR-	Right channel negative output
17	HP_LINE	Headphone, line input select pin, L – line input, H – headphone input
19	VDD	Power supply for other analog circuit
20	R_HP_IN	Right channel headphone input
21	OUTR+	Right channel positive output
22	SHUTDOWN	Shutdown mode select, L – shutdown enable, H – shutdown disable, normal work
23	R_LINE_IN	Right channel line input

Table 1: Gain vs. Gain0, Gain1 Logic Level

GAIN0	GAIN1	HP_SENSE	Mode	Gain
L	L	L	BTL	6dB
L	H	L	BTL	10dB
H	L	L	BTL	15.6dB
H	H	L	BTL	21.6dB
X	X	H	SE	4.1dB

Ordering Information

AA4006 ☐ ☐ - ☐

Circuit Type

Package
G: TSSOP-24 (EDP)

E1: Lead Free
G1: Green

TR: Tape and Reel

Package	Temperature Range	Part Number		Marking ID		Packing Type
		Lead Free	**Green**	**Lead Free**	**Green**	
TSSOP-24 (EDP)	-40 to 85°C	AA4006GTR-E1	AA4006GTR-G1	AA4006G	AA4006G-G1	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "E1" suffix in the part number, are RoHS compliant. Products with "G1" suffix are available in green packages.

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	6	V
Input Voltage	V_{IN}	-0.3 to V_{DD} + 0.3	V
Power Dissipation	P_D	Internally limited	
Package Thermal Resistance (Note 2)	θ_{JA}	65	$^oC/W$
Operating Junction Temperature	T_J	150	^oC
Storage Temperature Range	T_{STG}	-65 to 150	^oC
Lead Temperature (Soldering, 10 sec)	T_{LEAD}	260	^oC
ESD (Human Body Model)		2000	V
ESD (Machine Model)		200	V

Note 1: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operation is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

Note 2: Chip is soldered to 100mm^2 (4mm x 25mm) copper (top side solder mask) of 1oz. on PCB with 16 x 0.5mm vias.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	4.5	5.5	V
Operating Ambient Temperature	T_A	-40	85	^oC

Electrical Characteristics

$PV_{DD}=V_{DD}=5.0V$, Gain = 6dB @ BTL mode, 4.1dB @ SE mode, $T_A=25^oC$, f=1 kHz, 20 kHz Low pass filter, for SE mode, HP_SENSE=5.0V, for BTL mode, HP_SENSE=0V, unless otherwise specified.

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Quiescent Current		I_{DD}	SE mode, $V_{IN}=0$, $I_O=0$		3.5	7	mA
			BTL mode, $V_{IN}=0$, $I_O=0$		6.5	12	
Shutdown Current		I_{SD}	$V_{SHUTDOWN}=0V$		150	300	μA
High Logic Level	HP_SENSE, HP_LINE	V_{IH}		4.0			V
	GAIN0, GAIN1			3.0			V

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Electrical Characteristics (Continued)

V_{DD}=5.0V, Gain = 6dB @ BTL mode, 4.1dB @ SE mode, T_A=25°C, f=1kHz, 20kHz low pass filter, for SE mode, HP_SENSE=5.0V, for BTL mode, HP_SENSE=0V, unless otherwise specified.

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
High Logic Level	SHUTDOWN	V_{IH}		2.0			V
Low Logic Level	HP_SENSE, HP_LINE	V_{IL}				3.0	V
	GAIN0, GAIN1					2.0	V
	SHUTDOWN					0.8	V
Thermal Shutdown Temperature					165		°C
Hysteresis Temperature Window					35		°C
BEEP							
Input Amplitude		V_{BP}		2.5			V_{P-P}
Gain		G_{BP}	C_{BP}=0.47μF, f=1kHz, D=50% square wave form, V_{BP}=3.3Vp-p		0.3		V/V
SE mode							
Output Power		P_O	THD+N=1%, R_L=32Ω		90		mW
			THD+N=10%, R_L=32Ω		110		
			THD+N=1%, R_L=16Ω		180		
			THD+N=10%, R_L=16Ω		220		
Total Harmonic Distortion + Noise		THD+N	P_O=75mW, R_L=32Ω		0.03		%
Signal to Noise Ratio		S/N	P_O=75mW, R_L=32Ω		95		dB
Crosstalk		X_{TALK}	f=1kHz		-90		dB
Power Supply Rejection Ratio		PSRR	C_b=1μF, f=1kHz, V_{RIPPLE}=0.2V_{RMS}		60		dB
Output Noise		V_{NO}	f=20Hz to 20kHz, R_L=32Ω		20		$μV_{RM}$
BTL mode							
Output Offset Voltage			V_{IN}=0V, no load		±5	±25	mV
Output Power		P_O	THD+N=1%, R_L=3Ω		2.1		W
			THD+N=10%, R_L=3Ω		2.7		
			THD+N=1%, R_L=4Ω		1.8		
			THD+N=10%, R_L=4Ω		2.3		
			THD+N=1%, R_L=8Ω		1.2		
			THD+N=10%, R_L=8Ω		1.5		
Total Harmonic Distortion + Noise		THD+N	P_O=1W, R_L=4Ω		0.08		%
Signal to Noise Ratio		S/R	P_O=1W, R_L=4Ω		100		dB
Crosstalk		X_{TALK}	f=1kHz		-100		dB
Power Supply Rejection Ratio		PSRR	C_b=1μF, f=1kHz, V_{RIPPLE}=0.2V_{RMS}		70		dB
Output Noise		V_{NO}	f=20Hz to 20kHz, R_L=8Ω		18		$μV_{RM}$

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Typical Performance Characteristics
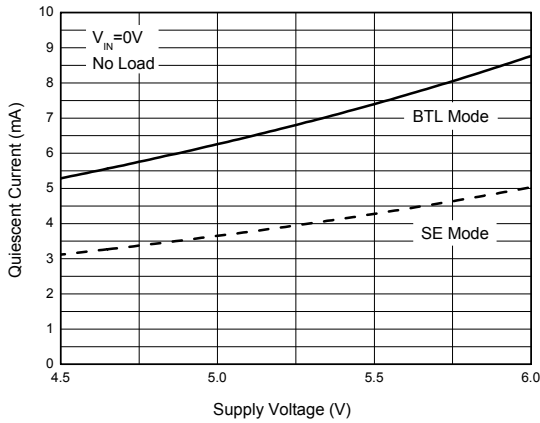
Figure 3. Quiescent Current vs. Supply Voltage
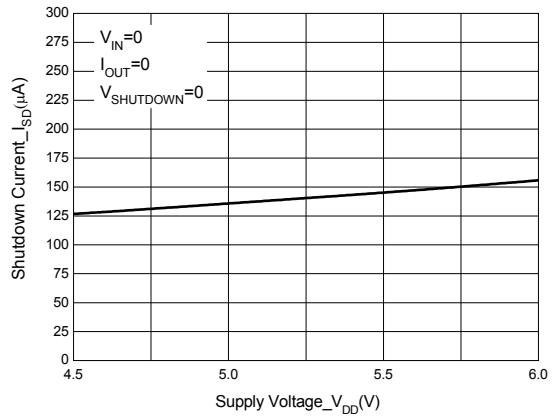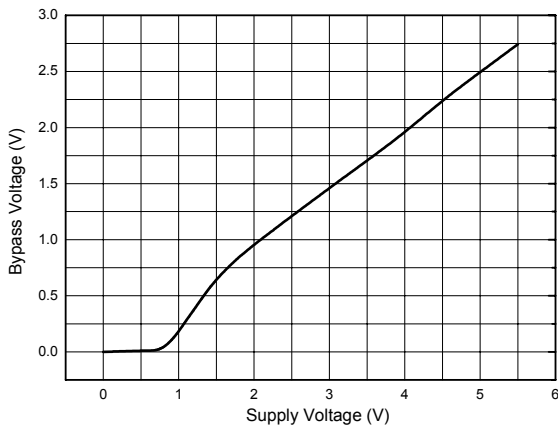

Figure 4. Shutdown Current vs. Supply Voltage

Figure 5. Bypass Voltage vs. Supply Voltage

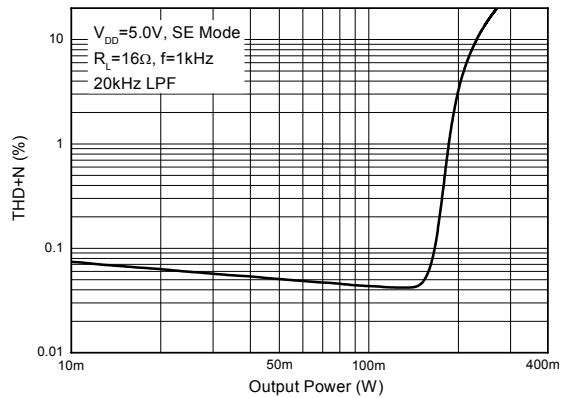Figure 6. THD+N vs. Output Power

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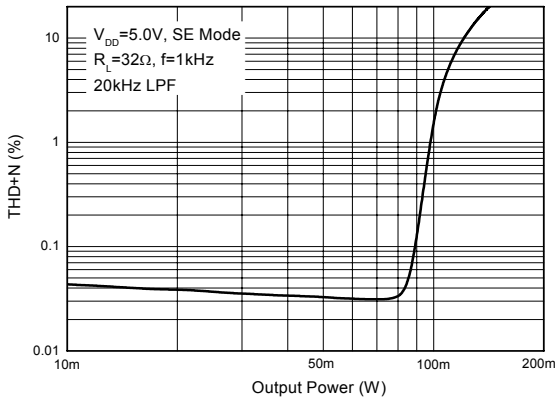
Typical Performance Characteristics (Continued)
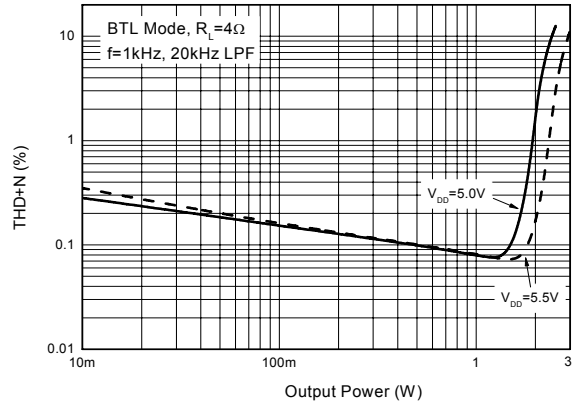
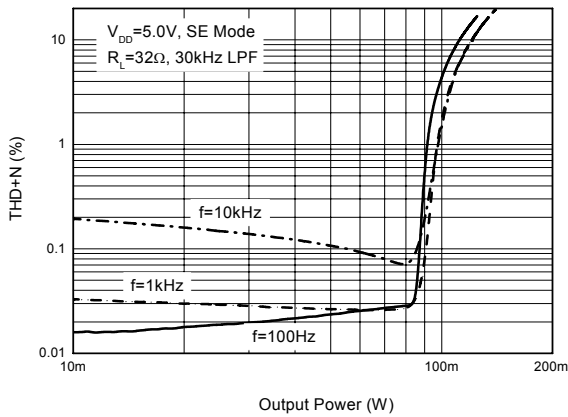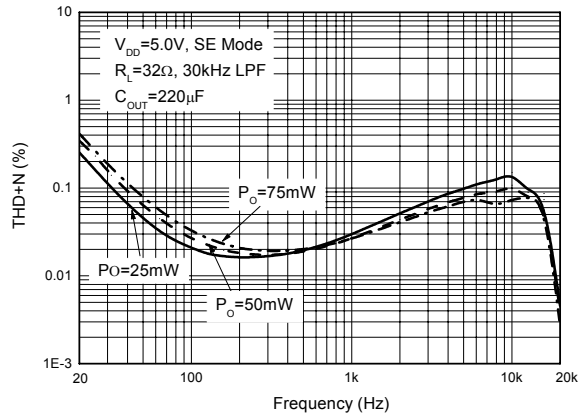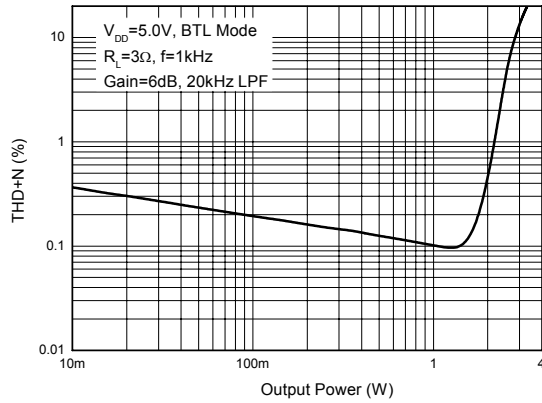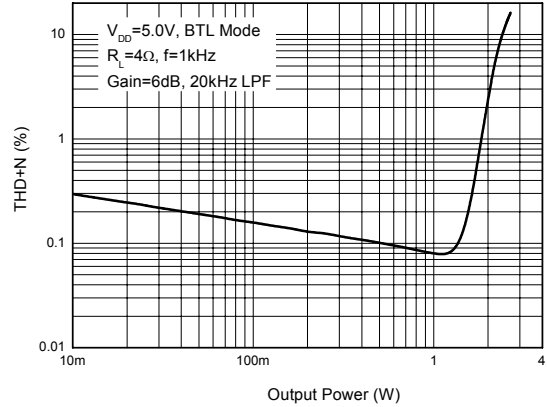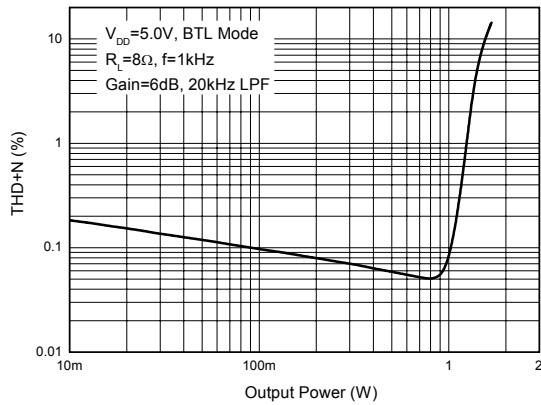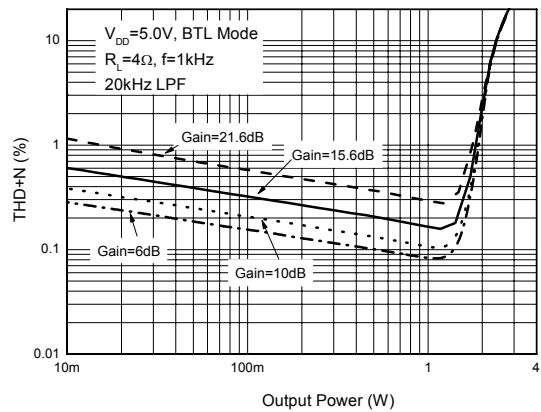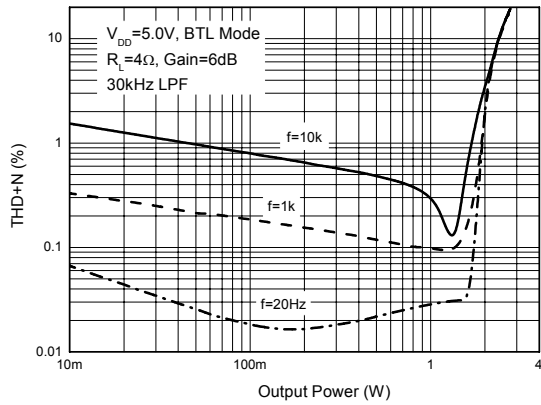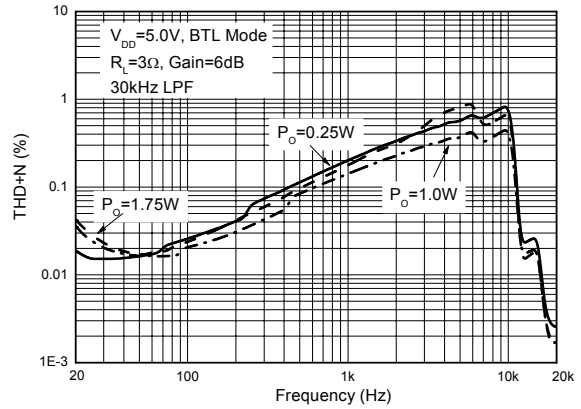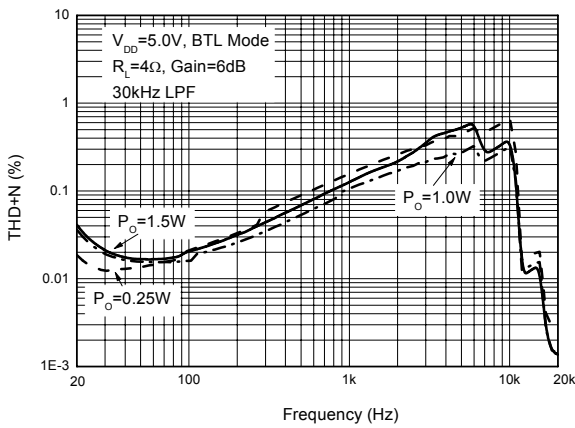Figure 7. THD+N vs. Output Power

Figure 8. THD+N vs. Output Power
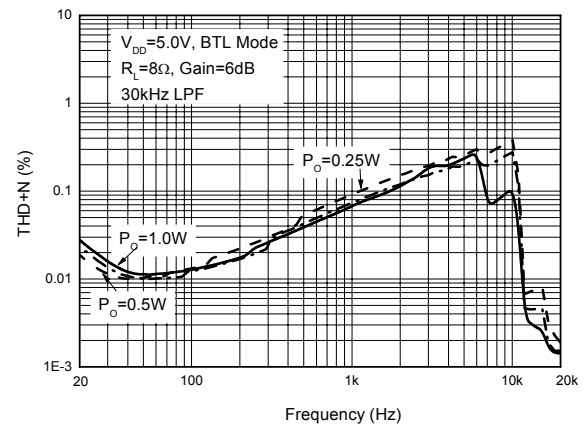
Figure 9. THD+N vs. Output Power

Figure 10. THD+N vs. Frequency

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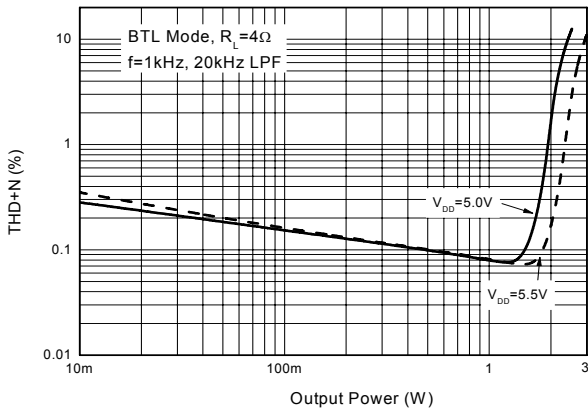## Typical Performance Characteristics (Continued)


Figure 11. THD+N vs. Output Power

Figure 12. THD+N vs. Output Power

Figure 13. THD+N vs. Output Power

Figure 14. THD+N vs. Output Power

2.7W Stereo Audio Power Amplifier with 4 Selectable Gain Setups and Input MUX AA4006

Typical Performance Characteristics (Continued)

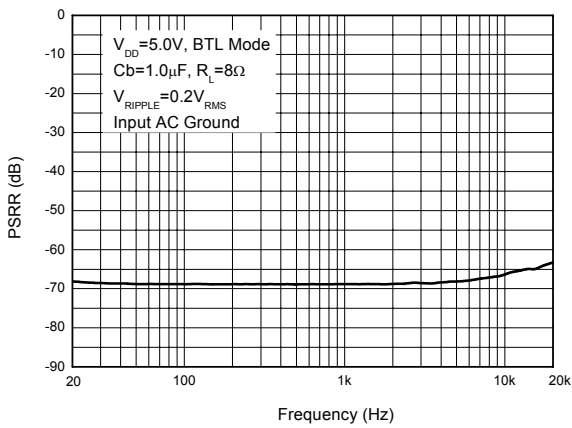Figure 15. THD+N vs. Output Power

Figure 16. THD+N vs. Frequency

Figure 17. THD+N vs. Frequency

Figure 18. THD+N vs. Frequency

Typical Performance Characteristics (Continued)

Figure 19. THD+N vs. Output Power
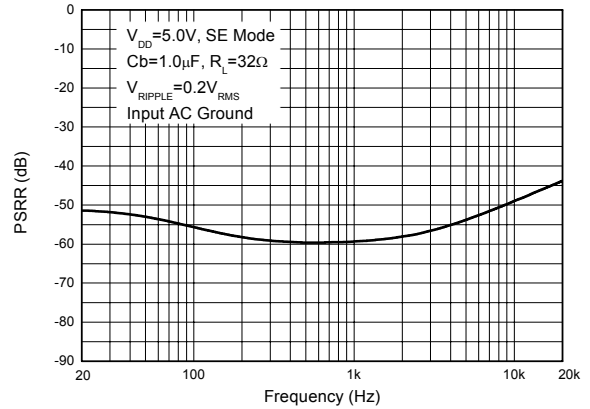
Figure 20. PSRR vs. Frequency
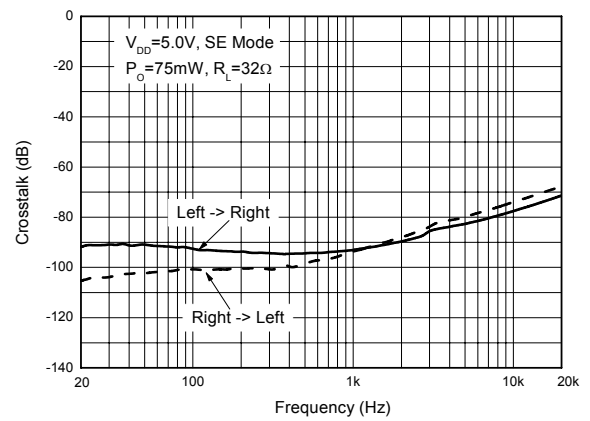

Figure 21. PSRR vs. Frequency

Figure 22. THD+N vs. Frequency

2.7W Stereo Audio Power Amplifier with 4 Selectable Gain Setups and Input MUX AA4006

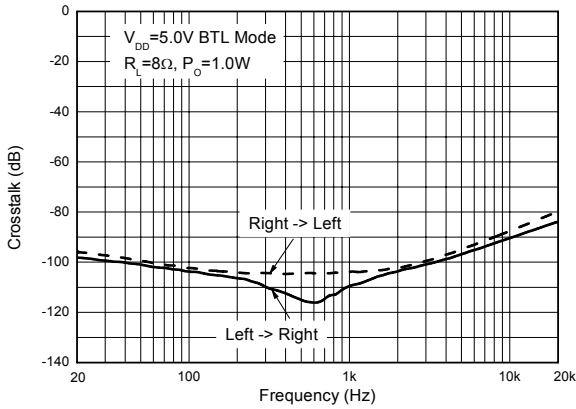## Typical Performance Characteristics (Continued)
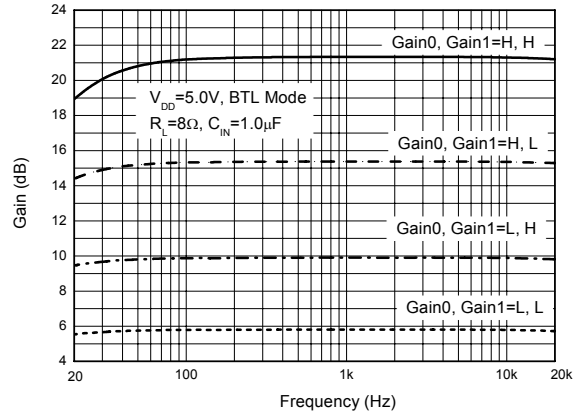

Figure 23. Crosstalk vs. Frequency
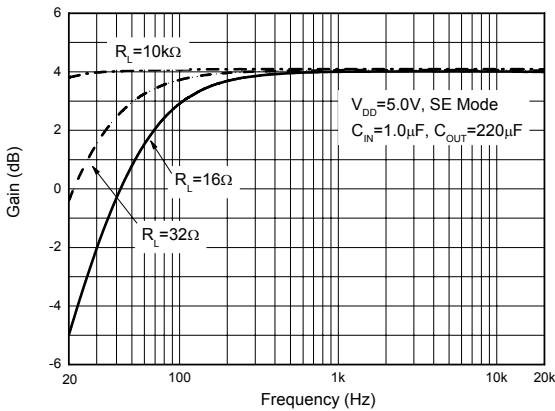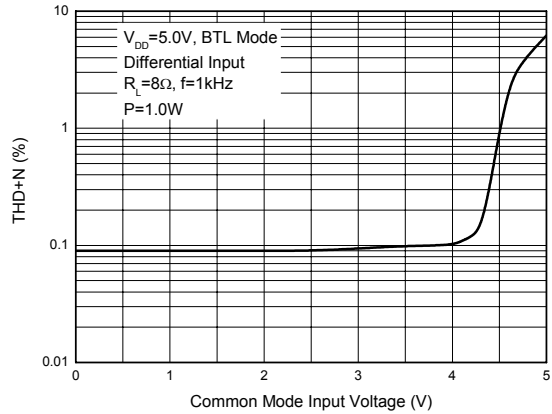

Figure 24. Gain vs. Frequency

Figure 25. Gain vs. Frequency

Figure 26. THD+N vs. Common Mode Input Voltage

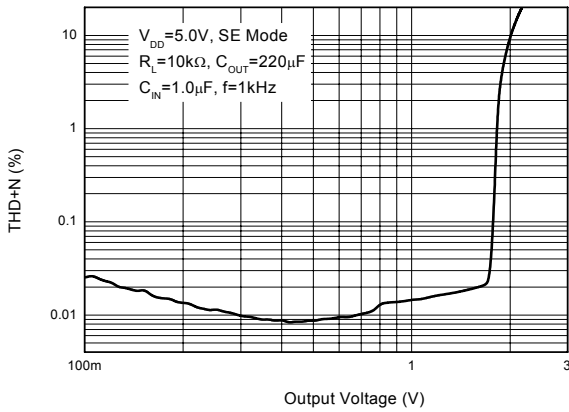## Typical Performance Characteristics (Continued)
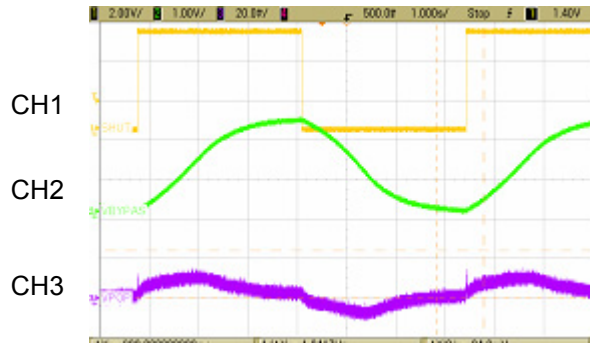

Figure 27. THD+N vs. Output Voltage

Figure 28. Pop Noise at SE Mode
(V_{DD}=5V, SE Mode, R_L=32Ω, C_b=1.0μF, C_{IN}=0.47μF,

C_{OUT}=220μF, CH1=$V_{SHUTDOWN}$, CH2=V_{BYPASS}, CH3=V_{OUT} at R_L)

Application Information

SE/BTL Mode, HP_SENSE Pin

The AA4006 can operate under 2 types of output configuration, SE (Single-Ended) mode and BTL (Bridged Tied Load) mode, determined by HP_SENSE pin's logic level. (Here is the discussion about left channel only, it can equally apply to right channel.)

When HP_SENSE pin is held low which sets the chip in BTL mode, both AMP1 and AMP2 are turned on. AMP2 has the same gain with AMP1 except 180 degree phase shift. Because the DC component (output bias voltage from AMP1 and AMP2, approx. 1/2 V_{DD}) between OUT+ and OUT- is canceled, there is no necessity to use DC block capacitors for speaker load. In BTL mode, output voltage swing across load is about 2 times that in SE mode, so there is about 4 times output power compared to SE mode with same load and input. (See Figure 29)

If applying high level to HP_SENSE pin which sets the chip in SE mode, AMP2 unit is turned off with high impedance. There is no current loop between OUT+ and OUT-, the speaker is naturally disabled without any hardware change. The output audio signal rides on bias voltage at OUT+ (output bias voltage from AMP1 and AMP2, approx. 1/2 V_{DD}), so it has to use a capacitor C_{OUT} to block DC bias voltage and couple AC signal to headphone load.

It is recommended to connect HP_SENSE to the headphone jack switch pin illustrated in Figure 29. When headphone plug is not inserted, the voltage of HP_SENSE pin is determined by voltage divider formed by R_L and R_{12}. For given resistors' value in Figure 29, R_L=1kΩ, R_{12}=100kΩ (Assuming V_{DD}=5.0V), DC voltage at HP_SENSE node is about 49.5mV. AC signal equals output amplitude of OUT+ through C_{OUT}, the maximum peak-peak voltage is no greater than V_{DD}, so the positive maximum voltage of HP_SENSE node will be no greater than 2.5V+49.5mV=2.55V(DC voltage plus AC voltage), which is less than HP_SENSE input high level minimum value (4.0V). That means the chip works in BTL mode reliably and there is no risk of operation mode switch between SE and BTL. When headphone plug is inserted, as the R_L is disconnected from R_{12}, the voltage of HP_SENSE pin is pulled up by R_{12} to V_{DD} sets the chip in SE mode.

HP_SENSE pin can also be connected to MCU I/O port directly to switch the operation mode between SE and BTL.

Input MUX, Single-Ended Input and Differential Input

The AA4006 offers the capability to use 2 individual stereo inputs: headphone input and line input. For a single-ended input, the common input terminal pins (L_IN, R_IN) should be connected to ground through a
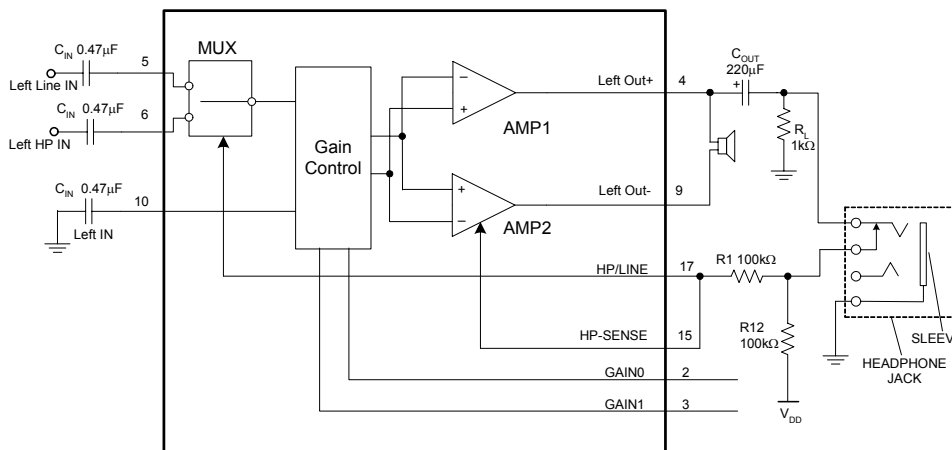

Figure 29. Input MUX and Output Configuration for Left Channel

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Application Information (Continued)

capacitor, also the size of C_{LIN} (C_{RIN}) has to be the same as C_{LLIN} (C_{RLIN}), C_{LHPIN} (C_{RHPIN}). Line input and headphone input are selected by switching HP_LINE pin. When HP_LINE is pulled high, the headphone input (L_HP_IN, R_HP_IN) is selected. When HP_LINE is held low, the line input (L_LINE_IN, R_LINE_IN) is selected. If the input signals are differential, only one stereo signal is permitted because share common input terminal pin (L_IN, R_IN), both headphone input and line input can be formed into differential pair with common input terminal. (See Figure 31)

With differential input configuration, the input coupling capacitors of differential pair can be removed if DC bias voltage of input source is within input common-mode voltage range, refer to Figure 26.

C_{IN}, C_{OUT}, C_b and C_S (Power Supply) Selection

Although there is no necessary to use input coupling capacitors in differential input if DC voltage of input is within common-mode input voltage range. The

AA4006 allows using input capacitors C_{IN} to accommodate different DC level between input source(like Audio D-A converter) and bias voltage (about 1/2 V_{DD}), especially in single-ended input mode which is popularly used in most applications. Input stage of AA4006 is illustrated as Figure 33, it is a full differential architecture, which consists of input resistor, R_{IN} and feedback resistor, R_{FB}.

In SE mode, pass-band gain is,

$$GAIN_{SE} = \frac{R_{FB}}{R_{IN}} \quad \text{..(1)}$$

In BTL mode, pass-band gain is,

$$GAIN_{BTL} = 2 * \frac{R_{FB}}{R_{IN}} \quad \text{..(2)}$$
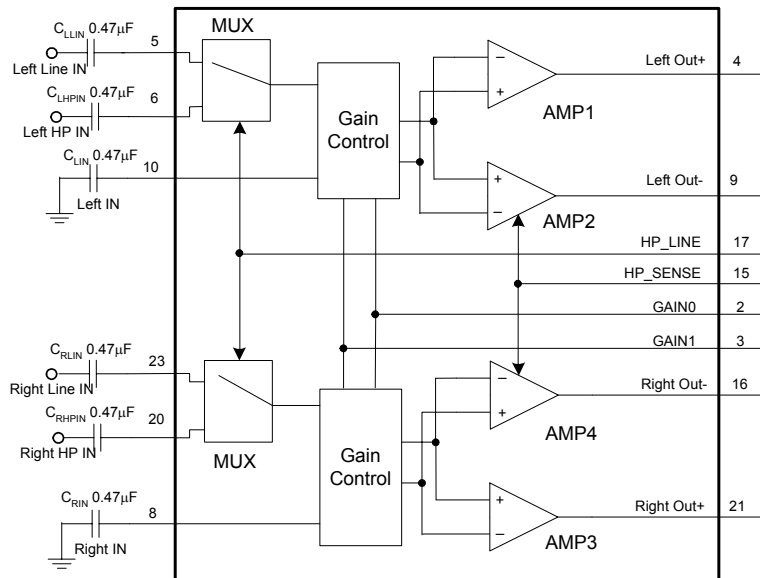
Figure 30. Single-Ended Input

Application Information (Continued)
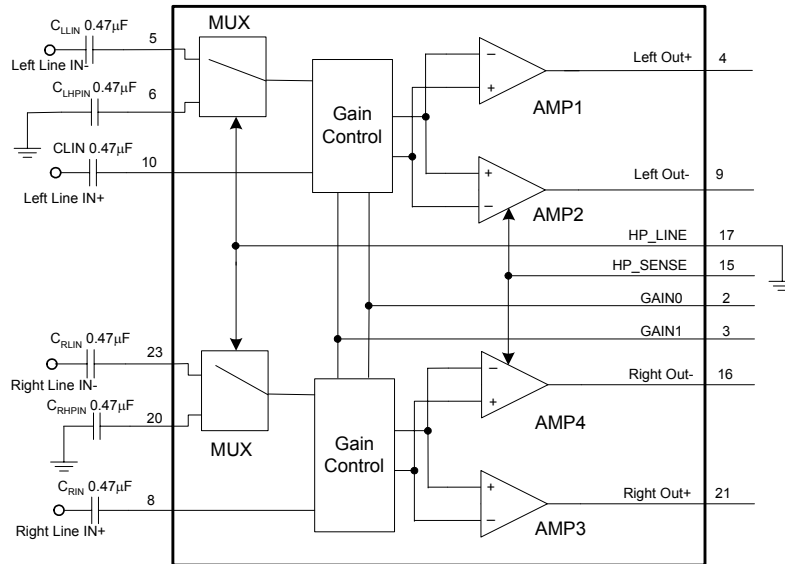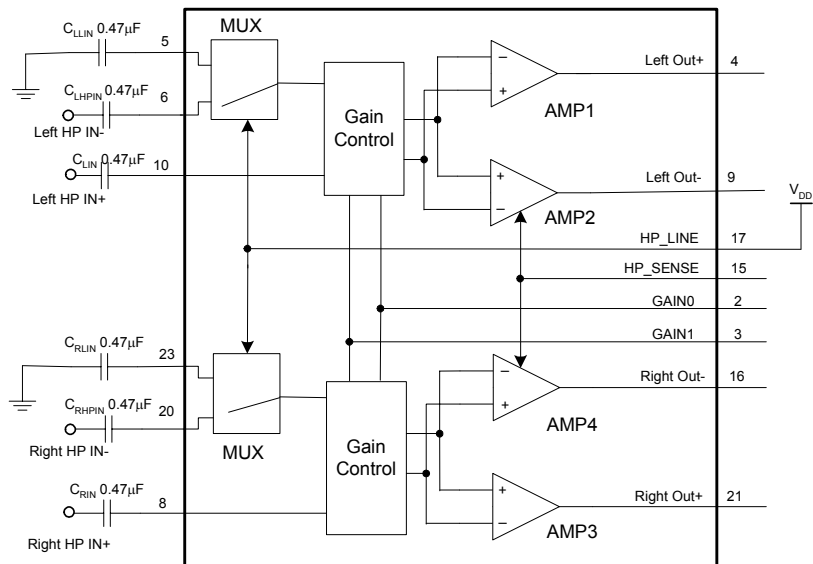
A) Using LINE_IN

B) Using HP_IN

Figure 31. Differential Input with Input Coupling Capacitors

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Application Information (Continued)
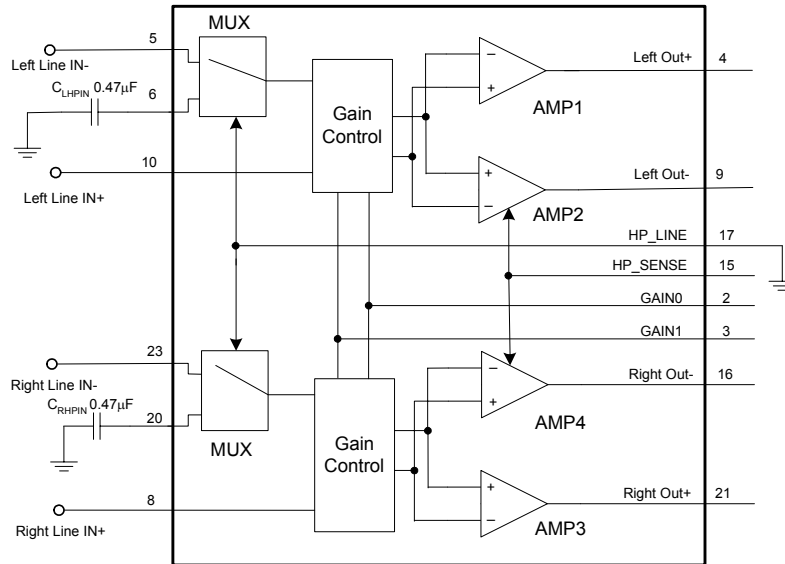
A) Using LINE_IN
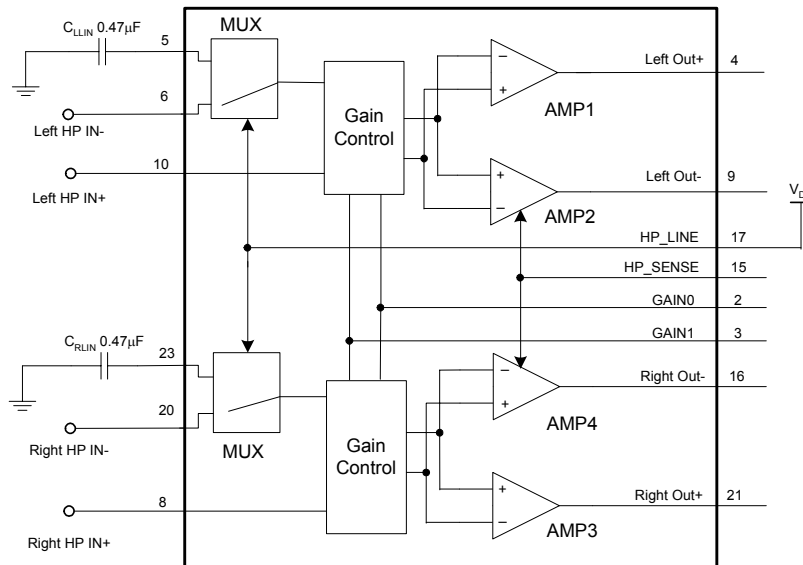
B) Using HP_IN

Figure 32. Differential Input without Input Coupling Capacitors

Application Information (Continued)

The typical input resistance, feedback resistance of AA4006 at each gain setting are showed in the table below.

GAIN0	GAIN1	HP_SENSE	GAIN (dB)	R_{IN} (Ω)	R_{FB} (Ω)
0	0	0	6	90	90
0	1	0	10	70	110
1	0	0	15.6	45	135
1	1	0	21.6	25	154
x	x	1	4.1	70	110

A) AA4006 Input Configuration with Input Capacitor

B) Classic Input Configuration with Input Capacitor

Figure 34. Input Configuration with Input Capacitor, C_{IN}
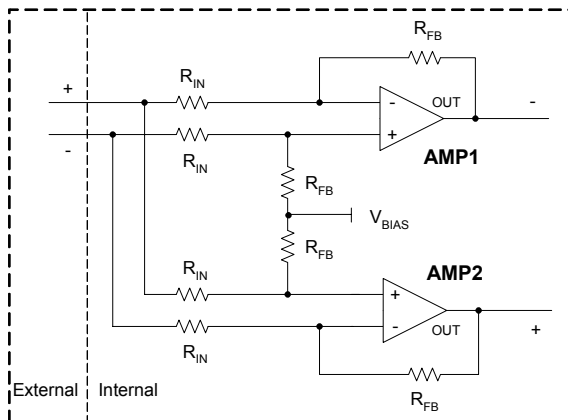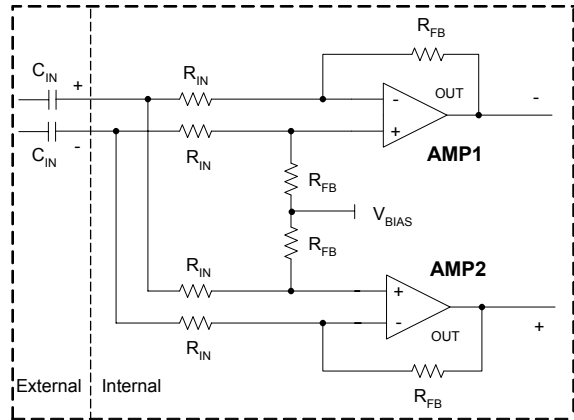
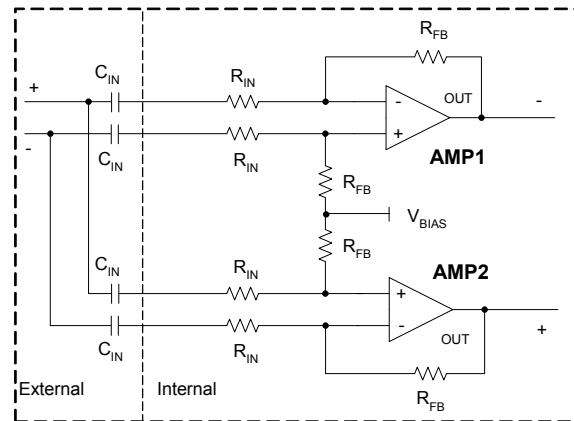

Figure 33. Full Differential Input Stage of AA4006

Input capacitors C_{IN} and input resistors R_{IN} form a first order High Pass Filter, which determines the lower corner frequency according to the equation below.

$$f_{CIL} = \frac{2}{2\pi R_{IN} * C_{IN}} \quad ....(3)$$

It is a little different from the classic equation according to Figure 34.

Input resistance varies with gain setting, also the absolute resistance of R_{IN} may drift $\pm$ 20% due to fab process. To ensure the minimum cut-off frequency within the audible range, the input capacitor (C_{IN}) has to be greater than 0.33μF. The low ESR ceramic capacitor of 0.47μF is recommended. See Figure 35 for frequency response using 0.47μF C_{IN}. However, using bigger size of C_{IN} will affect pop noise of AA4006.

If using an external resistor R_{EXT} in series with input capacitor C_{IN}, the closed-loop gain and cut-off frequency can be calculated by equations below.
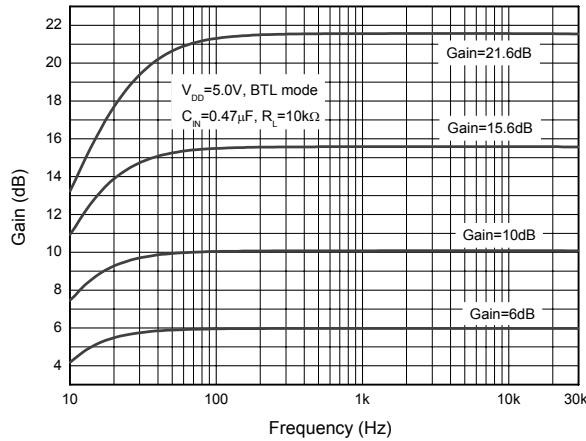
Application Information (Continued)

Figure 35. Frequency Response Using 0.47mF Input Capacitor

$$GAIN_{BTL} = 2 * \frac{R_{FB}}{2 * R_{EXT} + R_{IN}} \quad \text{..........................(4)}$$

$$f_{CIL} = \frac{2}{2\pi(2R_{EXT} + R_{IN})C_{IN}} \quad \text{...............................(5)}$$
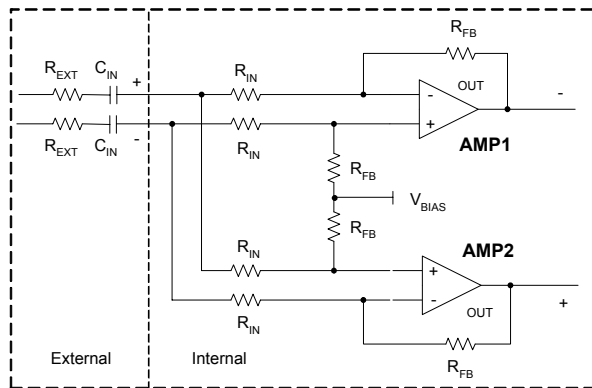

Figure 36. Using an External Resistor, R_{EXT} in Series with Input Capacitor, C_{IN}

Similarly, for output stage in SE mode, output capacitor (C_{OUT}) and headphone load (R_{HP}) also form a first order High Pass Filter, and its lower cut-off frequency is determined by equation 6.

$$f_{COL} = \frac{1}{2\pi R_{HP} * C_{OUT}} \quad \text{...(6)}$$

C_{OUT} (μF)	Headphone Load (Ω)	Lower Cut-off Frequency (Hz)
220	16	45.2
220	32	22.6
330	16	30
330	32	15

The purpose of the bypass capacitor (C_b) is to filter noise, reduce total harmonic distortion plus noise, and improve power supply rejection ratio performance. Tantalum or ceramic capacitor of 1.0μF with low ESR is recommended, and it should be placed as close as possible to the chip in PCB layout. This capacitor affects the pop noise performance furthest by changing the ramp of charge and/or discharge.

The below table shows output noise in each gain under the condition of 1.0μF bypass capacitor. Unit: μVrms.

			Filter: 22Hz ~ 22kHz	A- Weighted Filter
SE mode	C_{OUT}=220μF, R_L=16Ω		22	16
	C_{OUT}=220μF, R_L=32Ω		23	17
BTL mode	R_L= 4Ω	Gain0, Gain1 = 0, 0	18.5	13.5
		Gain0, Gain1 = 0, 1	23	17
		Gain0, Gain1 = 1, 0	32	24.5
		Gain0, Gain1 = 1, 1	46.5	37
	R_L= 8Ω	Gain0, Gain1 = 0, 0	19	14
		Gain0, Gain1 = 0, 1	24	18
		Gain0, Gain1 = 1, 0	33.5	25.5
		Gain0, Gain1 = 1, 1	52	39

Application Information (Continued)

For AA4006 power supply, it is better to use an individual power source generated from voltage regulator split from video, digital circuit units in system. For power supply bypass capacitor (C_S), it is recommended to use one low ESR electrolytic or tantalum capacitor from 4.7μF to 10μF in parallel with 0.1μF ceramic capacitor which is located close to the chip.

Shutdown

AA4006 has a shutdown feature to reduce power consumption during non-use operation. If apply low level to shutdown pin, output amplifiers, bias circuit will be turned off, the current drawn from V_{DD} is about 100μA. However, the Beep Detect circuitry is always ready to give alert on speaker load once apply any valid signal into BEEP_IN pin. The SHUTDOWN pin should be pulled high during normal operation, and it should never be left floating to prevent the unpredictable status of the chip.

However, the music signal will be output instantly once the SHUTDOWN pin is applied to logic level from low to high. When the SHUTDOWN pin changes from high to low, output will be present until bias voltage drops to approx 0.1V. See Figure 37 for time relationship between shutdown, bias voltage and output.

Optimizing Click/Pop Noise

The AA4006 includes optimized circuits to suppress Click/Pop noise during power up/power down transition.

In BTL mode, AA4006 can reduce most common mode signal also including Click/Pop noise due to symmetrical output.

In SE mode, optimized ramp for rise/fall edge of bias can significantly reduce Click/Pop noise generated by output capacitor (C_{OUT}) charge and/or discharge. Smoothing rise/fall edge of DC bias voltage is a quite important method. Another way is to prolong charge/discharge time which can shape power spectrum of output, and this makes some frequencies outside of the human audible range (20Hz to 20 kHz). So external components (including C_b, C_{IN}, C_{OUT} and headphone load) will affect pop noise performance. The recommended components are, C_b=1.0μF, C_{IN}=0.47μF, C_{OUT}=220μF, 32Ω for headphone load. Under given conditions, the maximum peak-peak voltage of pop noise is less than 15mV(See Figure 28). If using 16Ω headphone, the voltage of pop noise will decrease accordingly.

Beep Input

Beep input feature is used in computer system for alerting. A beep signal can be sent directly from a computer. If peak-peak voltage of beep signal applied to BEEP_IN pin (pin14) exceeds a certain voltage (typical 1/2 V_{DD}), the feature will be activated automatically, then AA4006 will be forced in BTL mode with the fixed gain of 0.3V/V, both LINE_IN and HP_IN are deselected, the logic level of HP_SENSE, HP_LINE, GAIN0, GAIN1 and SHUTDOWN is ignored. Once beep signal is removed from the chip, the AA4006 will return to the previous operation mode, gain settings.

The preferred beep signal is a square wave or pulse train, the preferred input is DC-coupled. If using AC-coupled, assuming beep input capacitor is 0.47μF, the input voltage is 3.3 Vp-p square wave, the beep signal should have a minimum of 10 cycles.

Power Dissipation, Efficiency and Thermal Design Consideration

For Class AB amplifiers, equation 7 is the basic equation of efficiency worked in BTL mode,

$$\eta = \frac{\pi V p}{4 V_{DD}} \quad ....(7)$$

Here V_P is output peak voltage across the load.

Thermal dissipation becomes major concern when delivering more power into speaker especially in BTL mode. The maximum allowed power dissipation can be calculated by equation below which is determined by thermal resistance of AA4006 package.

Application Information (Continued)

$$P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JA}} \quad ....(8)$$

Here T_{JMAX} is maximum operating junction temperature of 150°C, T_A is ambient temperature, θ_{JA} is thermal resistance from junction to ambient. For TSSOP-24(EDP) package, it is 65°C/W given in datasheet.

Assuming T_A is 25°C, the maximum allowed power dissipation is about 1.92W according to equation 8.

There is another equation about power dissipation which is determined by power supply voltage and load resistance under a certain application.

$$P_{DBTL} = 2 * \left(\frac{2V_P * V_{DD}}{\pi R_L} - \frac{V_P^2}{2R_L} \right) + V_{DD} * I_{DD} \quad ....(9)$$

The above equation expresses total power dissipation, dominated by dual channels, quiescent current. It is a quadratic equation with the negative coefficient of output voltage variation (V_P), there is always a maximum showed as below.

$$P_{DBTLMAX} = \frac{4V_{DD}^2}{\pi^2 R_L} + V_{DD} * I_{DD} \quad ....(10)$$

If power dissipation calculated by application is larger than the package permitted , it is necessary to use larger copper plane under the chip, or assemble an additional heat sink, or use forced-air cooling to keep ambient temperature around the chip low, or increase load resistance, or decrease power supply voltage.

For example, assuming V_{DD}=5.0V, speaker load R_{SP}=4.0Ω, stereo in BTL mode, the maximum power dissipation, includes 2 channels, plus quiescent power dissipation, dominated by quiescent current.

$$P_{DBTLMAX} = \frac{4V_{DD}^2}{\pi^2 R_L} + V_{DD} * I_{DD}$$

$$= \frac{4*5^2}{\pi^2*4} + 5.0*0.0065$$

$$= 2.56W$$

That is to say, to make sure AA4006 can output power into stereo 4Ω speakers continuously, the maximum ambient temperature should be no more than,

$$T_A = T_{JMAX} - \theta_{JA} * P_{DT}$$

$$= 150 - 65*2.56$$

$$= 16.4°C$$

The maximum power dissipation is achieved only when output power per-channel equals $2*V_{DD}2/\pi *R_{SP}$. If actual output power is not this data, power dissipation will be less than 2.56W.

When junction temperature exceeds about 165°C, OTSD feature will be enabled, that turns off output amplifiers to prevent damaging the chip. Once junction temperature drops lower than 130°C, the chip will work again automatically.

There is an exposed thermal pad on the bottom of the chip to provide the direct thermal path from die to heat sink. It is recommended to use copper on the surface of Printed Circuit Board (PCB) as heat sink. To dig some matrix regular holes under chip, remove mask of this area copper, and make sure to keep them contact well when soldering on PCB are also recommended.(See Figure 38)

Recommended PCB Layout

Using wide traces for power supply, BTL outputs to reduce power losses caused by parasitic resistance is recommended. It is also recommended to place bypass capacitor, and power supply decouple capacitor as close as possible to the chip.
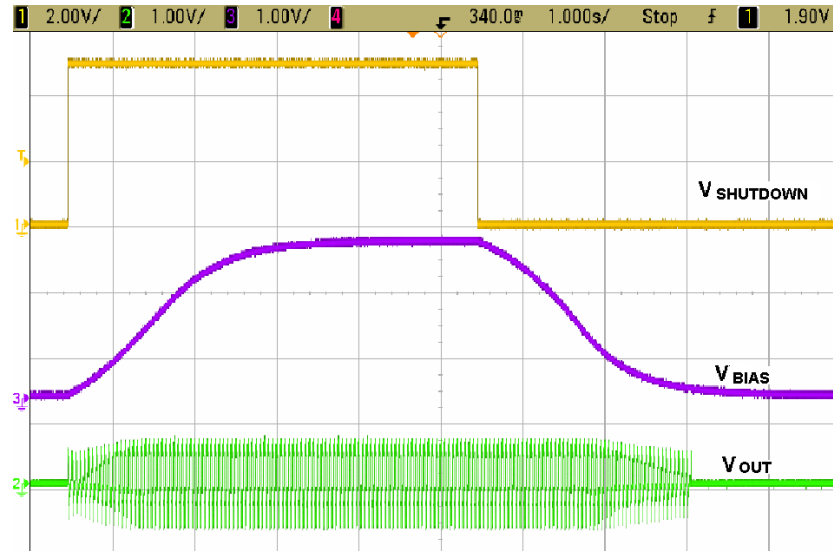
Application Information (Continued)

Figure 37. Time Chart for $V_{SHUTDOWN}$, V_{BIAS} and V_{OUT}
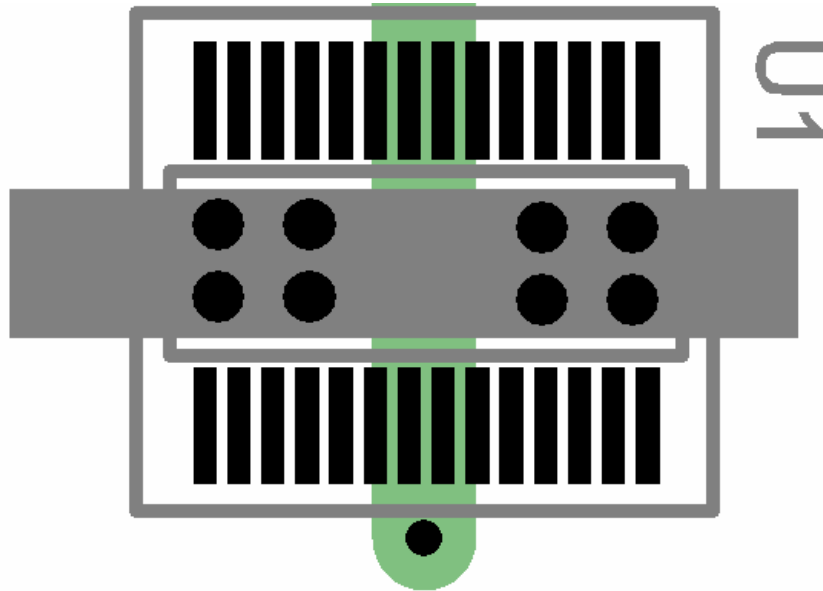
Figure 38. Recommended PCB Layout for Heat Sink

2.7W Stereo Audio Power Amplifier with 4 Selectable Gain Setups and Input MUX   AA4006
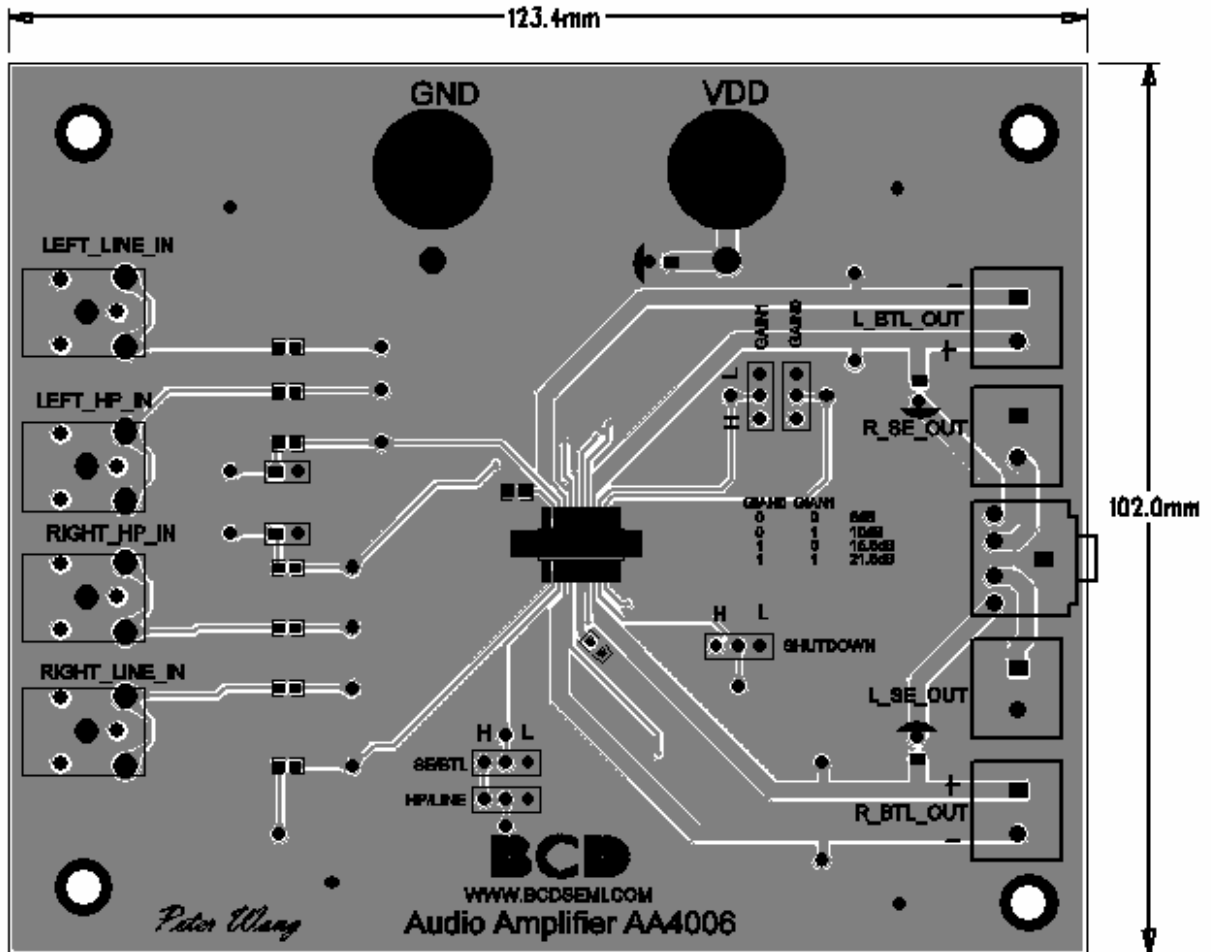
Application Information (Continued)

Figure 39. Top Route and Copper

2.7W Stereo Audio Power Amplifier with 4 Selectable Gain Setups and Input MUX AA4006
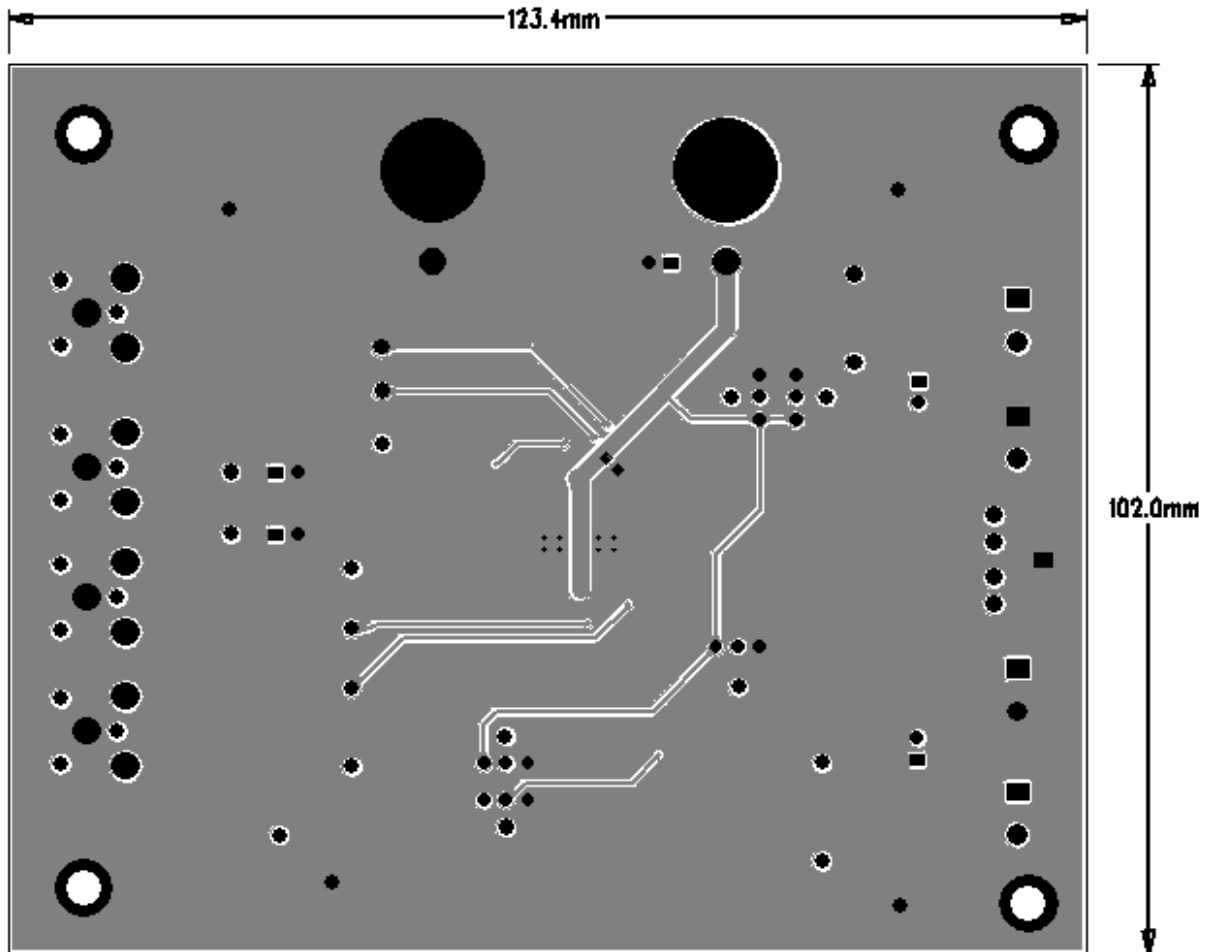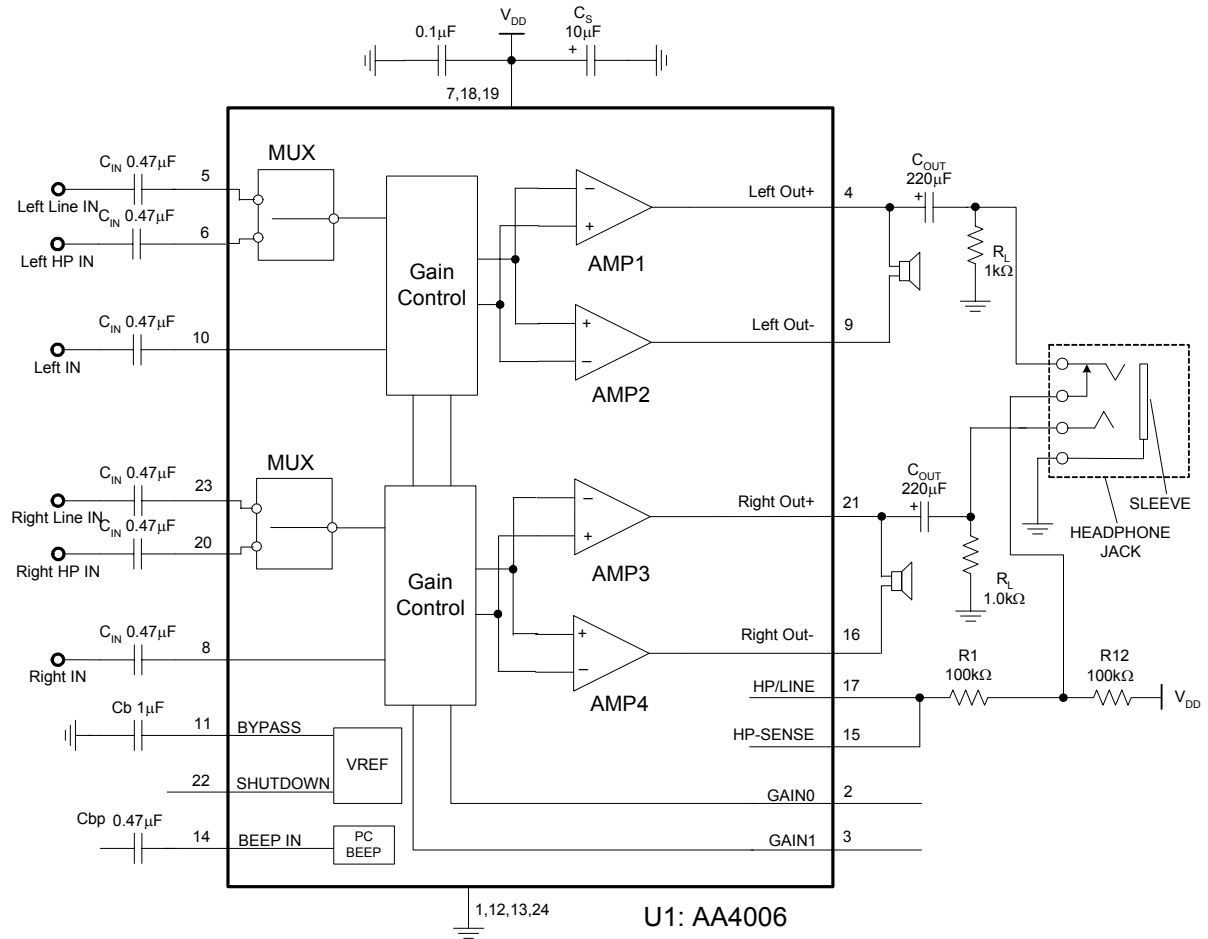
Application Information (Continued)

Figure 40. Bottom Route and Copper

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Typical Application

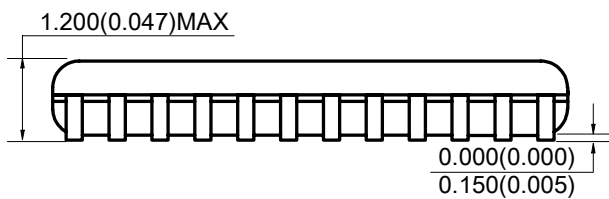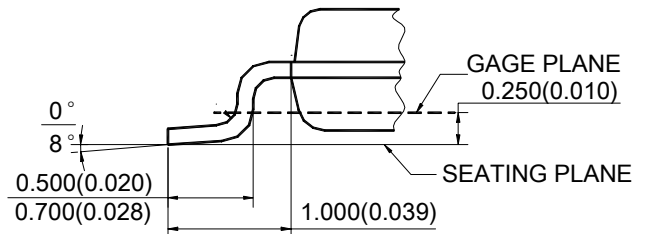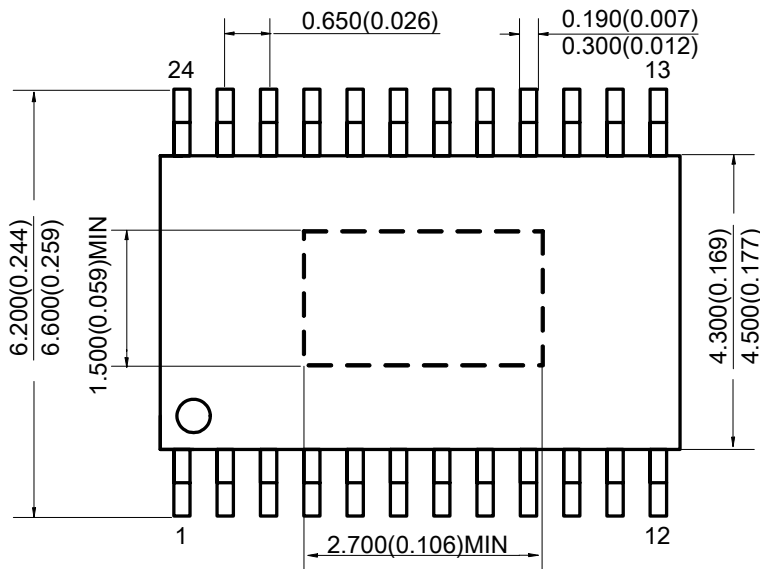Figure 41. Typical Application of AA4006

2.7W Stereo Audio Power Amplifier with 4 Selectable Gain Setups and Input MUX AA4006

Mechanical Dimensions

<div align="center">

TSSOP-24(EDP)   **Unit: mm(inch)**

</div>

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